Hall Ticket Number:

Code No.: 6125 M

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. I Year (ECE) I-Semester (Make Up) Examinations, March-2016

(Embedded Systems & VLSI Design)

Advanced Computer Organization

Time: 3 hours Max. Marks: 70

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

Part-A (10 X 2=20 Marks)

1. What are the inputs and outputs of the control unit?
2. What is the function of the program counter (PC) register? How many bits of data should PC hold?
3. You wrote a C program on your desktop, which is equipped with a 2GHz Pentium-4. Aftercompilation, you run the executable on the machine and found that it takes 2 seconds to run your program. You also found that the Pentium-4 has executed 4 billion instructions to run your program. What is the average CPI for the program?
4. Explain the principle of operation of cache memory.
5. What is the use of Peripheral Processor or Input/output Processor (IOP)?
6. What is the application of Device interface registers?
7. List out the performance parameters of pipeline processors.
8. What is microprogramming control unit?
9. Give the IEEE 32bit floating point format.
10. Draw the flow chart to explain the concept of programmed I/O technique.

Part-B (5 X 10=50 Marks)

11. a) Draw the flow chart for Booth's multiplication algorithm and illustrate the algorithm with an example. (5)
    b) A digital computer has a memory unit with a capacity of 16,384words, 40bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40 bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer. (5)

12. a) Define and describe virtual memory. What are its purposes, and what are the advantages and disadvantages of virtual memory systems? (5)
    b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K X 32.
        i. Formulate all pertinent information required to construct the cache memory.
        ii. What is the size of the cache memory? (5)

Contd –2--

13. a) What are the two principal design approaches for the control unit of a CPU? Describe each of them and discuss their advantages and disadvantages. If you were designing a family of high performance digital signal processors, which approach would you use, and why? (5)
    b) A computer as 16 registers, an ALU (arithmetic logic unit) with 32 operations and a shifter with eight operations, all connected to a common bus system.
        i. Formulate a control word for a microoperation.
        ii. Specify the number of bits in each field of the control word and give a general encoding scheme.
        iii. Show the bits of the control word that specify the microoperation $R_4 \leftarrow R_5 + R_6$ (5)

14. a) Given that many systems have a single bus which can be controlled by only one busmaster at a time (and thus the CPU cannot use the bus for other activities during I/O transfers), explain how a system that uses DMA for I/O can outperform one in which all I/O is done by the CPU. (4)
    b) Compare and contrast program-controlled I/O, interrupt-driven I/O, and DMA-based I/O. What are the advantages and disadvantages of each? Describe scenarios that would favor each particular approach over the others. (6)

15. a) Describe the M.J. Flynn's classification of parallel computer systems. (5)
    b) How are array processors similar to vector processors and how are they different? Explain the difference between fine-grained and coarse-grained array processors. Which type of array parallelism is more widely used in today's computer systems? Why? (5)

16. Describe the following concepts
    a) Memory models for multi processors organization (5)
    b) Dynamic scheduling in Instruction Level Parallelism (ILP) (5)

17. Suppose we increase the size of the IAS computer memory from 2^{12} words to 2^{15} words, keeping the word size unchanged at 40 bits:
    a) How will you change the binary format of instructions such that two instructions are still accommodated in a memory word? Is it possible to reassign opcodes to all IAS instructions? (3)
    b) What should the sizes of the following registers be: program counter (PC), accumulator (AC), multiplier quotient (MQ), memory buffer (MBR), instruction buffer (IBR), instruction registers (IR) and memory address (MAR)? (7)

*****